THIN SILICON MICROMACHINED STRUCTURES

Cross-Reference to Co-pending Patent Applications

This application is related to co-pending U.S. Patent Application Serial No. 09/748,488 [1100.1117101], entitled "SOI/GLASS PROCESS FOR FORMING THIN SILICON MICROMACHINED STRUCTURES", filed on date even herewith and incorporated herein by reference.

Field of the Invention

The present invention is related generally to semiconductor manufacturing and Micro Electro Mechanical Systems (MEMS). More specifically, the invention relates to methods for providing thin silicon micromachined structures.

Background of the Invention

Micro Electro Mechanical Systems (MEMS) often utilize micromachined structures such as beams, slabs, combs, and fingers. These structures can exhibit curvature due to internal stresses and doping gradients. The curvature can be a significant source of error in inertial sensors such as accelerometers, tuning forks, and gyroscopes. Many desired structures have a flatness design criteria that are difficult or impossible to achieve using current processes. In particular, silicon layers heavily doped with boron can have a significant curvature when used in suspended structures.

The aforementioned structures are often made starting with a silicon wafer substrate. A boron-doped silicon epitaxial layer is then grown on the silicon wafer substrate and is subsequently patterned in the desired shape. As is further described below, the boron is used as an etch stop in later processing to allow for easy removal of the silicon substrate, leaving only the thin boron-doped epitaxial layer.

At the interface between the boron-doped epitaxial layer and the silicon substrate, the boron tends to diffuse out of the epitaxial layer and into the silicon substrate. This depletes the epitaxial layer of some boron, and enriches the silicon substrate with boron. The epitaxial layer thus often has a reduced concentration of boron near the interface, which is sometimes called the "boron tail."

After the boron-doped silicon epitaxial layer has been grown to the desired thickness, the silicon substrate is often removed using an etchant that is boron selective. Specifically, the etchant will etch away the silicon substrate, but not the

boron-doped silicon epitaxial layer. One such etchant is a solution of ethylene diamine, pyrocatechol, and water (EDP). The etchant typically etches the silicon at a fast rate up to a certain high level boron concentration, at which point the etch rate significantly slows. This high boron concentration level is termed the etch stop level.

The boron concentration near the epitaxial layer surface having the boron tail may be lower than the etch stop level, allowing the etching to remove some of the epitaxial layer surface at a reasonable rate, stopping at the etch stop level of boron concentration beneath the initial surface. The resulting boron-doped structure, such as a beam, thus has two surfaces, the silicon side surface that has the boron tail and the airside surface that has a boron surface layer concentration substantially equal to the concentration in the bulk of the beam away from either surface. Thus, the opposing surfaces have different boron surface layer concentrations.

The building of a suspended element often includes using an epitaxially grown single-crystal silicon heavily doped with boron, for example, greater than ten to the twentieth atoms per cubic centimeter ($10^{20}/cm^3$). In some applications, this doped material may present problems. One problem is an intrinsic tensile stress, which, when the boron-doped layer is relatively thick, can produce severe wafer bow. This wafer bow is incompatible with some fabrication steps. Another problem is that the thickness of the epitaxial layer may be limited due to technological reasons, for example, deposition conditions. Yet another problem is that the Young modulus of the boron-doped material may be lower than that of silicon, and may not be well known and understood.

In addition, the intrinsic losses of the boron-doped material may be higher than those of low-doped silicon. In the lost wafer process, the final release of the mechanical structure is often performed using a long, wet-etching step, which can be based on ethylene-diamine-pyrocathacol (EDP) solution, which requires careful control to maintain industrial hygiene standards during manufacture. What would be desirable is a fabrication process that eliminates the need for highly doped silicon and does not require a wet-etching step using EDP.

Summary of the Invention

The present invention includes methods for making a thin silicon micromachined structure that can be used to make Micro Electro Mechanical Systems (MEMS). The thin silicon structure can be used in any number of applications including accelerometers, gyroscopes, and inertial sensing devices.

One illustrative method of the present invention uses a glass wafer or substrate and a thin silicon wafer having substantially planar first and second surfaces. The thin silicon wafer preferably has a thickness between about 10 and 100 microns or more. Recesses are formed in the glass wafer surface using standard photolithography techniques. After formation of the recesses, electrodes may be formed in the recesses and, in some embodiments, on the surface of the glass wafer, if desired. The electrodes within the recesses may serve as, for example, one plate of a capacitor used to sense distance to, or vibration of, a later added suspended structure disposed over the recess.

The silicon wafer can be bonded to the glass wafer or substrate over the recessed and non-recessed portions, using an appropriate method such as the anodic bonding, adhesives, heat bonding or any other suitable means. After bonding, a photolithography step can be performed on the back side of the now-bonded silicon wafer in order to define a shape on the silicon wafer. A DRIE process, or other suitable process, may then be used to etch the silicon, thus forming the silicon into the desired shape. Suitable shapes include tuning forks, combs, and cantilevered structures, among others. The silicon is preferably etched entirely through the silicon wafer.

In another illustrative embodiment of the present invention, a glass wafer or substrate and a thin silicon wafer with a metal layer on one surface thereof are provided. Like above, the glass wafer may be etched to form a recess or recesses in the glass wafer surface, and electrodes may be formed on the glass wafer surface and/or in the recesses. At least a portion of the metal layer on the silicon wafer is preferably patterned to coincide with the recesses in the glass wafer. The silicon wafer may then be bonded to the glass wafer surface, with the metal layer toward the glass wafer. After bonding, a photolithographic or other suitable process may be used

to etch the silicon into a desired pattern, preferably in the region above the patterned metal layer. The etchant is preferably selected to etch through the silicon but not the underlying metal layer. The metal layer thus act as an etch stop. The metal layer is believed to allow for sharper feature definition at the silicon-metalization layer interface, and also provides a barrier during the silicon etch step that may prevent gases in the recesses from escaping into the atmosphere, such as into a DRIE chamber. After etching of the silicon, the metal layer is preferably removed using standard etching techniques.

Brief Description of the Drawings

Figure 1A is a highly diagrammatic, longitudinal cross-sectional view of a silicon wafer and a glass wafer used in one process;

Figure 1B is a highly diagrammatic, longitudinal cross-sectional view of the glass wafer of Figure 1A after recesses have been etched in the glass wafer surface;

Figure 1C is a highly diagrammatic, longitudinal cross-sectional view of the glass wafer of Figure 1B after an electrode has been formed on the glass wafer surface in the recess areas;

Figure 1D is a highly diagrammatic, longitudinal cross-sectional view of the glass wafer of Figure 1C after the silicon wafer of Figure 1A has been bonded over the etched and non-etched surfaces of the glass wafer of Figure 1C;

Figure 1E is a highly diagrammatic, longitudinal cross-sectional view of the silicon wafer and glass wafer of Figure 1D after the silicon wafer has been etched;

Figure 2A is a highly diagrammatic, longitudinal cross-sectional view of a silicon wafer having a metalized surface and a glass wafer used in one embodiment process;

Figure 2B is a highly diagrammatic, longitudinal cross-sectional view of the glass wafer of Figure 2A after recesses have been etched into the glass wafer surface;

Figure 2C is a highly diagrammatic, longitudinal cross-sectional view of the glass wafer of Figure 2B after electrodes have been formed on the recessed surfaces;

Figure 2D is a highly diagrammatic, longitudinal cross-sectional view of the metalized silicon wafer of Figure 2A, and the metalized, recessed glass wafer of Figure 2C after bonding of the silicon wafer to the glass wafer;

Figure 2E is a highly diagrammatic, longitudinal cross-sectional view of the silicon wafer and glass wafer of Figure 2D after the silicon wafer has been etched through up to the silicon wafer metalized surface;

Figure 2F is a highly diagrammatic, longitudinal cross-sectional view of the silicon wafer and the glass wafer of Figure 2E after the metalized surface of the silicon wafer has been removed;

Figures 3A-3C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 1A-1E above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer; and

Figures 4A-4C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 2A-2F above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer.

Detailed Description of the Invention

Referring now to Figure 1A, a silicon wafer 20 having a first surface 28 and a second, substantially co-planar surface 26 is illustrated. Silicon wafer 20 is preferably undoped or substantially undoped (such as less than $10^{18}/cm^3$, and more preferably less than about $10^{17}/cm^3$, and has a thickness of about between 5 and 200 microns or more preferably between about 10 and 100 microns, depending on the application. A glass wafer or substrate 22 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 22 has a first surface 24 and substantially co-planar second surface 25.

To form an accelerometer, tuning fork, or gyroscope or the like, recesses are formed in the top surface 24 of the glass wafer. In Figure 1B, a first recess 30 and a second recess 34 are etched into the top surface 24 of the glass wafer 22. The first recess has a first recessed surface 32 and the second recess 34 has a second recessed surface 36. In some embodiments of the present invention, the recesses are used to form a capacitive gap for the detection of displacement of inertial electrodes, and are formed using standard etching techniques well known to those skilled in the art.

Figure 1C illustrates glass wafer 22 after electrodes 38 and 40 have been formed on the first recessed surface 32 and the second recessed surface 36. Although electrodes 38 and 40 are shown covering substantially all of the recesseD surfaces 32

and 36, it is contemplated that only a portion of the recessed surfaces 32 and 36 may be covered, if desired. In addition, the second recess 34 has an electrode tab or ear 42 extending nearer the unrecessed surface of the glass wafer 22. This may or may not be required, depending on the application. Metal electrodes 38 and 40 are preferably formed using techniques well known to those skilled in the art. In one illustrative embodiment, the electrodes are titanium-platinum or gold-based electrodes.

Figure 1D illustrates silicon wafer 20 and glass wafer 22 after the first surface 28 of silicon wafer 20 has been bonded to glass wafer 22. As may be seen from inspection of Figure 1D, silicon wafer 20 has been bonded over both recessed and nonrecessed portions of glass wafer 22. In one embodiment, silicon wafer 20 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding, etc.

Figure 1E illustrates silicon wafer 20 after an etch has been performed on the second surface 26 of silicon wafer 20. When forming a typical device, such as an accelerometer, tuning fork, or gyroscope, several etched regions 44 may be formed. Preferably, the silicon etch extends through the silicon wafer 20 and into recesses 30 and 34 of the glass wafer 22. The silicon is preferably etched using standard silicon etching procedures, such as a Deep Reactive Ion Etch (DRIE) process. Preferably, a standard photolithography process is used to define the desired structural shapes into the silicon wafer 20. Examples of suitable shapes include, but are not limited to, cantilevered beams, suspended beams, combs, tuning forks, etc.

In another illustrative embodiment, and referring now to Figure 2A, a silicon wafer 120 is provided. As above, the silicon wafer has a thickness of about between 5 and 200 microns or more preferably between about 10 and 100 microns, depending on the application. A metal layer 129 is then provided on one surface of the silicon wafer 120. The metal layer 129 may be provided as part of the originally supplied silicon wafer or it may be deposited or otherwise formed thereupon using conventional methods. One suitable metal for the formation of metal layer 129 is chromium on oxide, although other metals or alloys may be used.

Figure 2B illustrates a glass wafer 22 after recesses 30 and 34 have been formed, as previously discussed above with respect to Figure 1B. Figure 2C

illustrates glass wafer 22 after formation of electrodes 38 and 40, as previously discussed with respect to Figure 1C. Preferably, the metal layer 129 is patterned so that the remaining metal corresponds to or is otherwise defined to fit within recesses 30 and 34.

In Figure 2D, the metalized silicon wafer 120 is shown bonded to the glass wafer 22, with the metal layer 129 situated adjacent the glass wafer 22. One method for bonding the silicon wafer 120 to the glass wafer 22 is anodic bonding. A by-product of some anodic bonding processes is the release of oxygen. As can be seen, the cavities formed between the recesses 30 and 34 and the silicon wafer 120 may collect the oxygen released during the anodic bonding process, and thus may have an increased concentration thereof.

Figure 2E shows the silicon wafer 120 after a pattern has been etched therein to form the desired structure. The etching preferably includes a suitably selective etching technique that etches through silicon wafer layer 120, but not through metal layer 129. Standard lithography techniques can be used to define the series of recesses, channels, or holes 144 through the silicon wafer 120, but not through the metal layer 129. The metal layer 129 thus may serve as an etch stop layer. It has been found that by providing an etch stop layer, sharper feature definition at the interface of the silicon wafer 120 and the metal layer 129 can be achieved, resulting in more precise feature definition in the resulting silicon structure.

Another benefit of providing metal layer 129 is that a seal or barrier is provided to prevent gasses from escaping from recesses 30 and 34 into the atmosphere during the silicon etching process. This can be particularly important when the silicon wafer 120 is etched using an etching process that relies at least in part on the gas composition in the surrounding atmosphere, such as a DRIE etching process. The release of gases, such as oxygen which as described above may be collected in the recesses 30 and 34 during the anodic bonding process, can effect the effectiveness and/or controllability of some etching processes, such as a DRIE etching process.

Figure 2F illustrates the silicon wafer 120 and glass wafer 22 after the metal layer 129 has been removed. The metal layer 129 may be removed in recess areas 30

and 34 using techniques well known to those skilled in the art. In one example, an etchant capable of removing the metal layer 129, but not the silicon wafer 120, may be applied to the silicon wafer recesses 144. The etchant may thus dissolve metal layer 129. In a preferred embodiment, the etchant is capable of removing metal layer 129, but does not remove electrodes 38 and 40. Figure 2F illustrates the resulting product having a silicon layer 120 formed into a suitable structure and bonded to glass wafer 22.

Figures 3A-3C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 1A-1E above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer. Figure 3A illustrates a silicon wafer 200 having a first surface 202 and a second, substantially co-planar surface 204. A first recess 206 and a second recess 208 are etched into the first surface 202 of the silicon wafer 200, as shown. Preferably, the first recess 206 and the second recess 208 do not extend all the way through the silicon wafer 200. In some embodiments, the recesses are used to form a capacitive gap for the detection of displacement of inertial electrodes, and are formed using standard etching techniques well known to those skilled in the art. A glass wafer or substrate 210 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 210 has a first surface 212.

Figure 3B illustrates the glass wafer 210 after electrodes 214 and 216 have been formed on the first surface 212 of the glass wafer 210. Figure 3C illustrates silicon wafer 200 and glass wafer 210 after the first surface 202 of the silicon wafer 200 has been bonded to the first surface 212 of glass wafer 210. In one embodiment, silicon wafer 200 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding, etc. The remaining processing steps may be similar to that shown and described above with respect to Figure 1E.

Figures 4A-4C are highly diagrammatic, longitudinal, cross-sectional views similar to that shown in Figures 2A-2F above, but with the recess or recesses formed in the silicon wafer rather than the glass wafer. Like in Figure 2A, a silicon wafer 220 having a first surface 222 and a second, substantially co-planar surface 224 is

illustrated. A first recess 226 and a second recess 228 are etched into the first surface 222 of the silicon wafer 220, as shown. Preferably, the first recess 226 and the second recess 228 do not extend all the way through the silicon wafer 220. A glass wafer or substrate 230 is also provided, preferably formed from a material such as a Pyrex™ Corning Type No. 7740. The glass wafer 230 has a first surface 232.

As shown in Figure 4B, a metal layer 236 is provided on the recessed surface of recess 226, and a metal layer 238 is provided on the recessed surface of recess 228. The metal layers 236 and 238 are preferably deposited or otherwise formed thereupon using conventional methods. One suitable metal for the formation of metal layers 236 and 238 is chromium on oxide, although other metals or alloys may be used. Figure 4B also illustrates the glass wafer 230 after electrodes 240 and 242 have been formed.

Figure 4C shows silicon wafer 220 and glass wafer 230 after the first surface 222 of the silicon wafer 220 has been bonded to the glass wafer 230. In one embodiment, silicon wafer 220 is bonded using an anodic bonding process. However, other bonding techniques may be used including adhesives, heat bonding, etc. The remaining processing steps may be similar to that shown and described above with respect to Figures 2E-2F.

While the above illustrative embodiments use a silicon wafer and a glass wafer, it is contemplated that any suitable material system may be used. For example, rather than using a silicon wafer, it is contemplated that any suitable material system may be used including for example, GaAs, silicon-nitride, etc. Likewise, rather than using a glass wafer, any fairly rigid substrate may be used.

Numerous advantages of the invention covered by this document have been set forth in the foregoing description. It will be understood, however, that this disclosure is, in many respects, only illustrative. Changes may be made in details, particularly in matters of shape, size, and arrangement of parts without exceeding the scope of the invention. For example, while the above illustrative embodiments include a silicon wafer bonded to a glass wafer or substrate, other material systems may be used. The invention's scope is, of course, defined in the language in which the appended claims are expressed.